Implementation of Single Carrier Packet Transmission with Frequency Domain Equalization

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Abstract—**Single-carrier (SC) transmission using frequency domain equalization (FDE) is one of the candidates for the next generation mobile communication systems expected to deliver high-speed and high-quality packet data services. Fast synchronization is critical for the performance of packet transmission systems. In this paper, a robust timing synchronization scheme for SC-FDE packet transmission is presented and its implementation is discussed. The proposed scheme uses an integration process to find the optimum timing of the guard interval (GI). An SC-FDE packet transmission system is implemented on a FPGA and its performance is analyzed through experimental data.**

Index Terms—**Single-carrier, packet transmission, frequency domain equalization, timing synchronization**

I. INTRODUCTION

As the next generation mobile communication systems will have to support mainly data services, high-speed packet transmission will be one of the key technologies. For high-speed data transmission, single carrier (SC) systems using frequency domain equalization (FDE) based on the minimum mean square error (MMSE) criterion are attractive as they are very efficient in combating the effects of frequency selective fading while maintaining the low peak to average power ratio (PAPR) advantage of SC schemes over OFDM[1],[2].

In packet transmission systems, synchronization is a major problem. Due to the fact that data is sent in short duration bursts, little or no tracking is necessary but the system must perform acquisition every time a packet is received. In order to minimize the latency associated with this, high speed synchronization schemes are required. Furthermore, with the use of high-performance error correcting codes, data transmission is possible even with low signal to noise ratios (SNR), therefore, synchronization schemes that can achieve synchronization in this kind of conditions are highly desirable.

The problem of timing synchronization for SC-FDE systems has been investigated in [3],[4],[5]. In [3], the parameters that have to be synchronized are analyzed and some solutions are given but the bit error rate (BER) performance is not investigated. In [4], the problem of synchronization is analyzed but continuous transmission is assumed. In [5], synchronization for SC-FDE is considered based on the similarities with OFDM and a different preamble sequence is used. In

this paper, we present a timing synchronization scheme that uses the self-correlation of one sequence and an integrator to find the optimum timing of the GI that contains all the distinguishable paths.

The rest of this paper is organized as follows. Section II describes the implemented SC-FDE system. In Sect. III the proposed synchronization scheme is presented and some design parameters are discussed. The performance of the implemented SC-FDE packet transmission system is evaluated in Sect. IV through experimental data. Conclusions are given in Sect. V.

II. SYSTEM OVERVIEW

Figure 1 shows the block diagram of the considered SC-FDE system. The data to be transmitted is divided into N symbol blocks and a guard interval (GI) is added per block by copying the last N_g symbols. A block containing the pilot sequence used for channel estimation is multiplexed into the transmit signal. A preamble is inserted in the front of the packet as illustrated in Fig. 2. A root raised cosine (RRC) filter is used in both transmitter and receiver to form a raised cosine (RC) filter.

In the receiver, after the GI is removed the received signal $r(t)$ is transformed into the frequency domain through the FFT operator and $R(n)$ is obtained. One tap FDE is applied to this signal as

$$\hat{R}(n) = w(n)R(n). \qquad (1)$$

In the above expression, $w(n)$ denotes the MMSE equalization weight and is given by [6]

$$w(n) = \frac{H^*(n)}{|H(n)|^2 + 2\sigma^2} \qquad (2)$$

where $H(n)$ is the n-th frequency component of the channel transfer function, $(\cdot)^*$ and σ^2 denote the complex conjugate operation and the noise variance, respectively.

$H(n)$ and σ are variables that have to be estimated. The adopted channel estimation technique is given in [7]. The block diagram of the channel estimation block is depicted in Fig. 3. The Chu sequence [8] was employed as the pilot
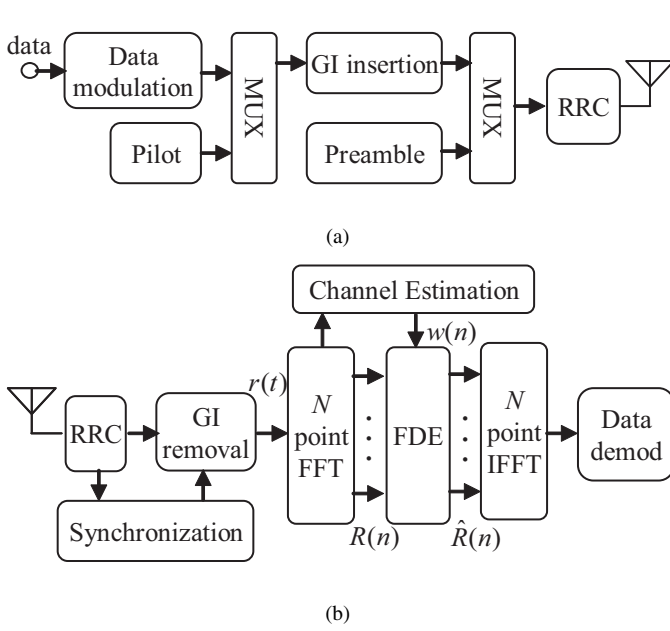
Fig. 3. Channel estimation block diagram.

(a)

(b)

Fig. 1. Transmission system block diagram: (a) transmitter, (b) receiver.

Fig. 2. Packet structure.

Fig. 4. Equalizer circuit block diagram.

signal because it has constant amplitudes in both time and frequency domain. When the pilot signal is received, after the FFT operator it is reverse modulated to obtain an estimation of the channel transfer function. To reduce the influence of the noise delay-time domain windowing is used[9]. IFFT is applied on the channel transfer function to obtain the channel impulse response and the part outside the GI is replaced with zeros. Through another FFT an improved estimates of the channel transfer function $\hat{H}(n)$ are obtained. The noise power is estimated as given in [10] by using the part outside the GI from the channel impulse response. Finally, $\hat{H}(n)$ and the estimated σ^2 are used to compute $w(n)$ as given in Eq. 2.

The described equalizer was implemented on a FPGA. The block diagram of the circuit is illustrated in Fig. 4. The Coordinate rotation digital computer (CORDIC) algorithm [11],[12] was employed for the division operator used to compute the equalization weights. Two division modules that compute the real and imaginary parts in parallel were used because they share the denominator. Reverse modulation can be processed the same way as equalization, but instead of the weights the pilot frequency components are used. The FDE module was implemented using two parallel complex multipliers because the weights are stored in a dual port memory.

III. TIMING SYNCHRONIZATION

Timing synchronization can be divided into two phases, symbol synchronization and frame synchronization[13]. For the case of a SC-FDE system symbol synchronization means finding the optimum timing to downsample the output of the RRC filter. Frame synchronization means finding the
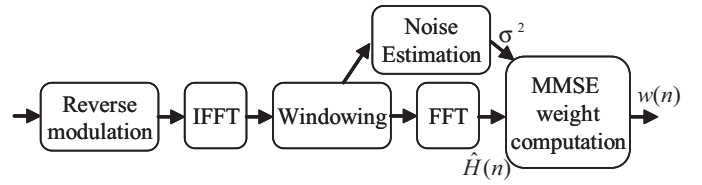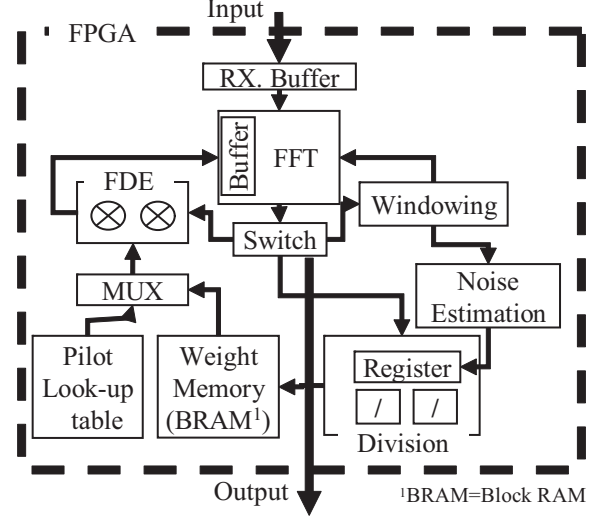
optimum timing of the FFT window which is equivalent to finding the timing of the GI. For synchronization a preamble sequence with very good self-correlation characteristic such as M sequence is employed. The synchronization block in Fig. 1 contains a correlator which outputs the correlation value of the received signal as shown in Fig. 5 (a). In this example a 8-paths channel and a 8 symbols GI is considered. For an intuitive understanding of the proposed scheme, the mechanism of frame synchronization is explained first.

Conventional schemes set the frame synchronization timing when the correlation value exceeds a certain threshold V_{th} or by searching for its peak. Due to multipath fading, the gain of each path has a large dynamic range, therefore, it is difficult to lock the synchronization timing on the first path by using either method.

In the proposed scheme, an integration process is used and the receiver takes into account the entire impulse response of the channel, including the response of the RC filter, to set the timing of the GI such that all the distinguishable paths are contained inside the GI. This is accomplished as follows.

The output of the correlator is inserted into an integrator with a width equal to that of the GI. The integrator output $i(t)$ is expressed as

$$i(t) = \sum_{k=0}^{N_g-1} c(t-k) \qquad (3)$$

where $c(t)$ is the correlator output. By searching for the maximum of $i(t)$, the GI position containing all the paths can be found as illustrated in Fig. 5 (b). The integrator can be
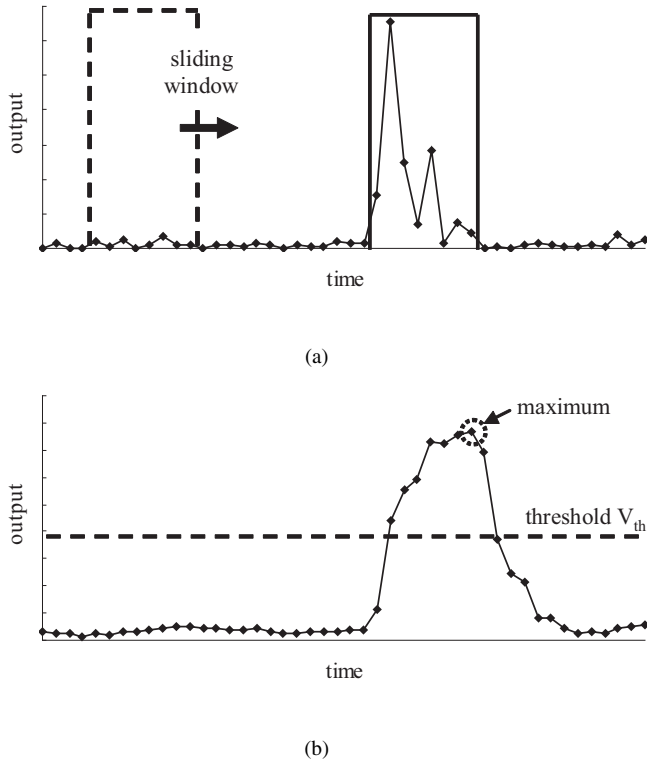
Fig. 5. Proposed scheme: (a) correlator output, (b) integrator output.

regarded as a sliding window of width N_g within which all the samples are added. The window marked with the thick line shows the position where the frame synchronization is locked. The search for the maximum starts when the integrator output exceeds a threshold and continues for N_g-1 samples. Because the gains of all the paths are added there is a much bigger margin for setting a threshold, thus, decreasing the probability of false alarm or a packet not being detected.

Symbol synchronization can be found by performing a search in parallel for every oversampled output of the receive filter such that symbol and frame synchronizations can be locked at the same timing. The block diagram of the synchronization module for the proposed scheme in shown in Fig. 6. The number of parallel correlators is equal to the oversampling factor of the RRC filter, denoted here by S.

Every output sample from the RRC filter $r(t_{over})$ is fed to one of the parallel correlators. The input $c_{in}(t)$ of the i-th correlator is given as

$$c_{in,i}(t) = r(t + i) \tag{4}$$

where $t = \lfloor t_{over}/S \rfloor$ and $i = t_{over} \mod S$. The output of the i-th correlator c_i is inserted into the i-th integrator. The output of the i-th integragor is given as

$$i_i(t) = \sum_{k=0}^{N_g-1} c_i(t - k). \tag{5}$$

A search for the maximum among all $i_i(t)$ starts when $i_i(t) \geq V_{th}$ for any i and yields the synchronization timing t_{sync}. This
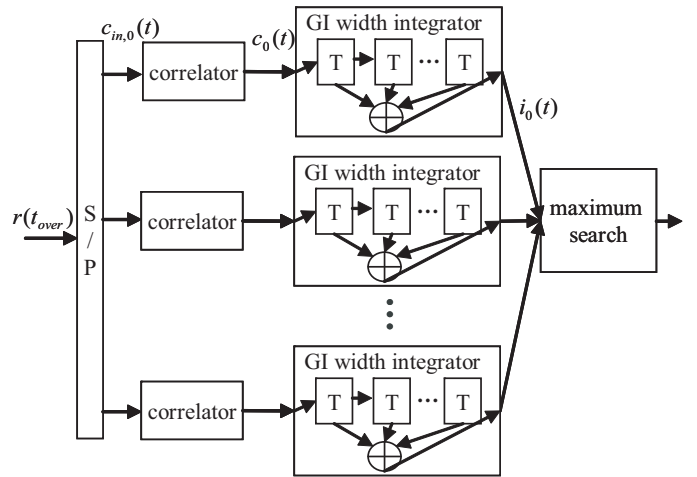

Fig. 6. Synchronization module block diagram.

can be described as

$$t_{sync} = T_s + S \tag{6}$$

where T_s satisfies the following condition

$$i_{T_s \mod S}(\lfloor T_s/S \rfloor) = \max\{i_i(t)\}. \tag{7}$$

By using the preamble correlation and the integration process the proposed scheme takes into account the entire channel impulse response including the RC filter response and finds the optimum synchronization timing such that the whole channel response is contained inside the GI.

The influence of the preamble length on the system performance was evaluated through computer simulation. The simulation parameters are listed in Table I. The packet structure is depicted in Fig. 2. Two channel models are considered, a 16-paths ideal one where all the paths arrive at integer symbol intervals and a 14-paths random one in which the path delays are uniformly distributed inside one symbol duration.

The performances for preamble lengths of 63 and 127 symbols were compared as shown in Fig. 7. The case of 127 symbols preamble shows significantly better performance for $E_b/N_0 > 20[dB]$ in both channels. The degradation for the case of 63 symbols is due to the fact that there is not enough process gain to clearly distinguish the tails of the channel impulse response. For the case of 127 symbols in the ideal channel there is no performance degradation compared to the ideal synchronization case.

TABLE I
SIMULATION PARAMETERS.

Modulation	QPSK
FFT points	128
GI	16 symbols
Channel model	multipath Rayleigh fading
Preamble	M sequence

IV. PERFORMANCE EVALUATION

A. Experimental Conditions

To evaluate the performance of the proposed scheme an SC-FDE packet transmission system was implemented. The
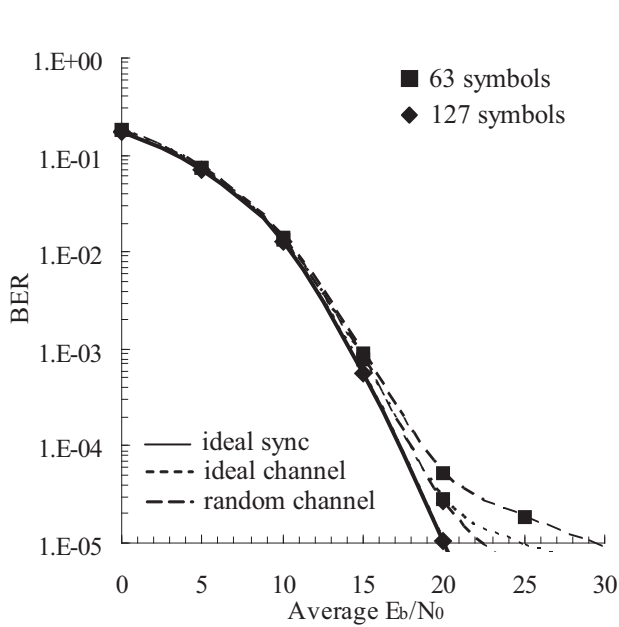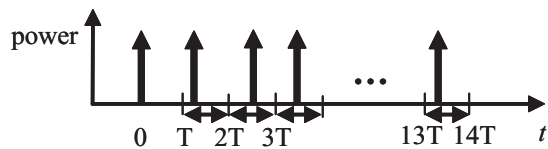
Fig. 7. Preamble length comparison.

Fig. 8. Random channel delay profile.

block diagram of the transmission system is shown in Fig. 9. For the implementation of the baseband signal processing 2 FPGAs were used, a Virtex4 SX55 and a Virtex4 LX200 as depicted in Fig. 10. The experimental parameters are listed in Table II. The degradation induced by the analog circuit was measured using a 1 path timely invariant channel and found to be constant 2.5dB. This is compensated for in the performance evaluation.

TABLE II
EXPERIMENTAL CONDITIONS.

Modulation	QPSK
FFT points	128
GI	16 symbols
Mobile terminal speed	1.5km/h
Packet composition	Preamble/Pilot 1 block/Data 7 blocks
Root raised cosine filter	65 taps, 8x oversampling
Roll off factor α	0.2
Data rate	3.125 Msps
Total number of packets sent	163830

B. BER Performance

The performance of the proposed synchronization scheme was evaluated using a one symbol spaced 8 paths uniform power delay profile and compared to the simulation and the case of ideal synchronization (cunning). The results are shown in Fig. 11. The performance degradation due to synchronization is negligible even for low E_b/N_0 values. The performance
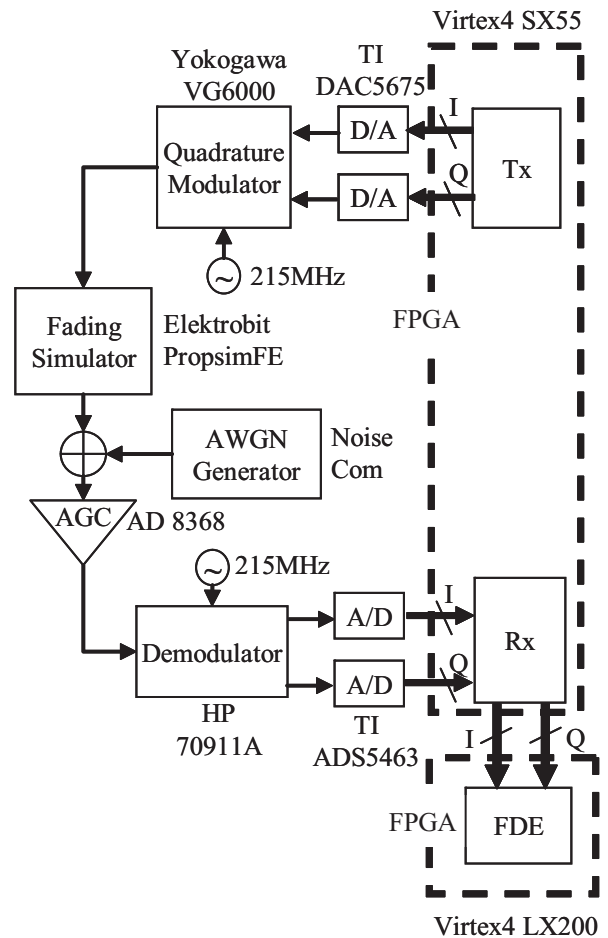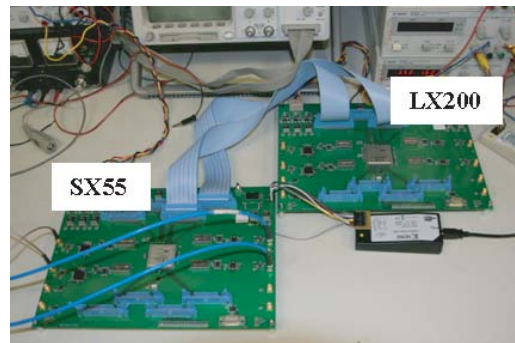

Fig. 9. Transmission system block diagram.

Fig. 10. Baseband implementation boards.

degradation in the $E_b/N_0 > 15$[dB] range compared to the simulation is considered to be due to the direct current (DC) offset contained in the received signal generated by the down-converter.

The impact of the RRC filter roll off factor α on the system performance was investigated using channels with a delay profile that extends almost as long as the GI. Two 14 paths uniform power delay profile channels were considered. An ideal channel in which the delay between paths are exactly one symbol and a channel in which the delays are not integer symbol intervals. The relative delays for this channel are

listed in Table III. Note that the symbol's length is 320ns. The measurement results are shown in Fig. 12. $\alpha = 0.2$ achieves better performance due to the fact that the proposed synchronization scheme locks the synchronization in the point where the received power is biggest. For the case when $\alpha = 0.2$ the side lobes of the raised cosine filter are bigger so the probability of finding the optimum synchronization timing is higher. When $\alpha = 0.5$ the side lobes of the raised cosine filter are smaller and they are more difficult to distinguish from the side lobes of the preamble correlation, thus, the probability of finding the optimum timing becomes smaller. In both cases there is a performance degradation in the $E_b/N_0 > 15$[dB] range due to IBI caused by the filter response extending outside the GI. Comparing the results of the two channels, it is clear that the degradation is greater in the case of the random channel. The cause is the impulse response of the paths coming at random intervals that extends more outside the GI.

TABLE III
RELATIVE PATH DELAYS.

Path number	Delay range (ns)	Path number	Delay range (ns)
0	0	7	2300
1	480	8	2670
2	720	9	2900
3	1100	10	3300
4	1350	11	3620
5	1680	12	3980
6	2050	13	4200

Fig. 12. Impact of α.

Fig. 11. BER performance.

the performance of the proposed scheme was evaluated with experimental data. It was shown that the proposed synchronization scheme induces a negligible performance degradation compared to the ideal synchronization. The impact of the roll off factor α was also investigated and it was found that $\alpha = 0.2$ achieves better performance than $\alpha = 0.5$.
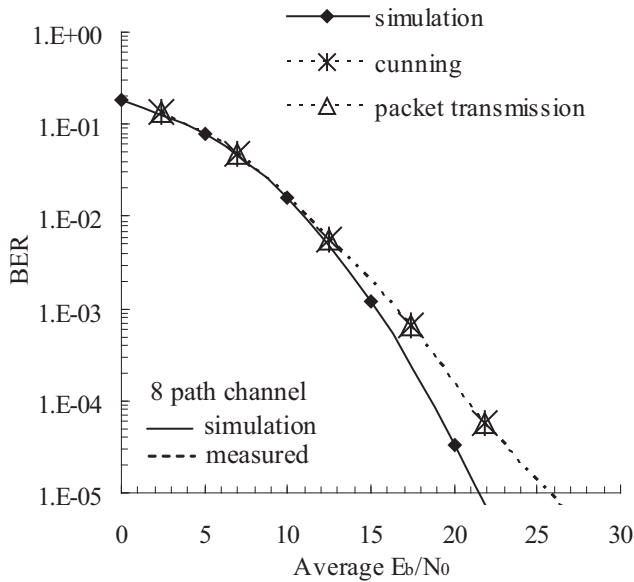
V. CONCLUSION

In this paper, a timing synchronization scheme suitable for SC-FDE packet transmission systems was presented. The proposed scheme takes into account the channel response as a whole and finds the optimum GI timing. An entire SC-FDE packet transmission system was implemented and
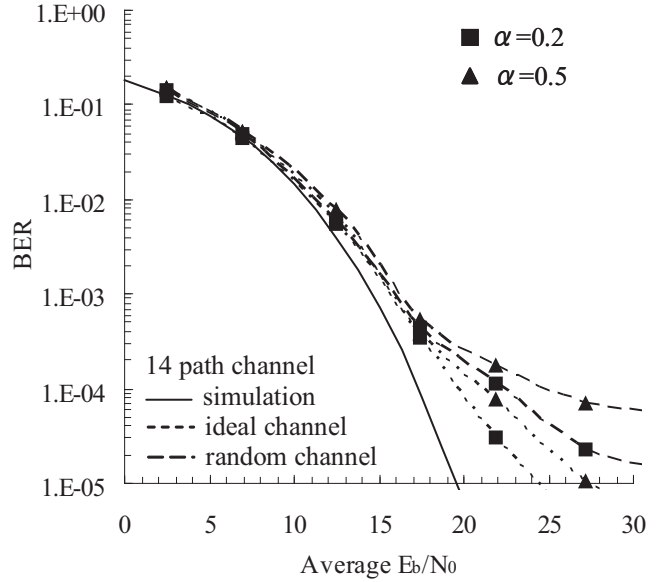
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