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PAPER

Performance Comparison of Overlap FDE and Sliding-Window Chip Equalization for Multi-Code DS-CDMA in a Frequency-Selective Fading Channel

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SUMMARY Recently, overlap frequency-domain equalization (FDE) based on minimum mean square error (MMSE) criterion which requires no guard interval (GI) insertion was proposed for signal transmission using multi-code direct sequence code division multiple access (DS-CDMA) in a frequency-selective fading channel. Another promising equalization technique is time-domain sliding-window chip equalization (SWCE). In this paper, the bit error rate (BER) performances achievable with overlap FDE and SWCE are compared. It is shown that, by extending the fast Fourier transform (FFT) block size, overlap FDE can achieve almost the same BER performance as SWCE with much less computational complexity than SWCE.

key words: *overlap FDE, sliding-window chip equalization (SWCE), DS-CDMA*

1. Introduction

Direct sequence code division multiple access (DS-CDMA) has been adopted as the wireless access technique in the 3rd generation (3G) mobile communication systems [1]. In 3G DS-CDMA, coherent rake combining is used to exploit the moderate frequency-selectivity of the channel to obtain the path diversity gain. However, if the coherent rake combining is applied to broadband DS-CDMA, the bit error rate (BER) performance degrades due to the strong inter-path interference (IPI) [2], [3]. The use of frequency-domain equalization (FDE) based on the minimum mean square error (MMSE) criterion can take advantage of the channel frequency-selectivity and can significantly improve the BER performance [4]–[6]. The conventional FDE requires the insertion of guard interval (GI) to avoid the inter-block interference (IBI). Unfortunately, the transmission throughput is reduced. Furthermore, when the maximum time delay of the channel exceeds the GI length, the BER performance degrades due to the IBI. In [7] and [8], overlap FDE which requires no GI insertion was presented. Overlap FDE can effectively suppress the residual IBI after FDE. It provides higher throughput than the conventional FDE at the expense of increased computational complexity [9].

Another promising equalization technique which requires no GI insertion is time-domain sliding-window chip equalization (SWCE) based on MMSE criterion [10], [11]. It was shown [10] that SWCE can achieve better BER performance than the coherent rake combining.

In both overlap FDE and SWCE, the received DS-CDMA signal stream is divided into a sequence of M-chip blocks and then, equalization is applied over an extended block of N_c chips centering the M-chip block of interest ($M \leq N_c$). After equalization, an M-chip block is picked up. Important design parameters for overlap FDE and SWCE are M and N_c. To the best of our knowledge, how the choice of M and N_c affects differently the BER performance achievable by overlap FDE and SWCE has not been fully understood. In this paper, we present the BER performance and computational complexity comparison between overlap FDE and SWCE in multi-code DS-CDMA signal transmission in a frequency-selective fading channel. We will show that, by extending the fast Fourier transform (FFT) block size N_c, overlap FDE can achieve almost the same BER performance as SWCE with much less computational complexity.

The remainder of this paper is organized as follows. Section 2 presents the system model of multi-code DS-CDMA signal transmission using overlap FDE and SWCE. In Sect. 3, the BER performance comparison and computational complexity comparison are presented by computer simulation. Section 4 offers some conclusions.

2. Multi-code DS-CDMA Using Overlap FDE and SWCE

2.1 System Model

Figure 1 shows the system model of the multi-code DS-CDMA signal transmission. At the transmitter, the binary information sequence is data-modulated and then converted into U parallel symbol streams $\{d_u(n)\}$ by a serial/parallel (S/P) converter. The u-th ($u = 0 \sim U-1$) symbol stream is spread by the orthogonal spreading code $c_u(t)$ with spreading factor SF ($SF \geq U$). U parallel chip sequences are added and multiplied by a scrambling sequence $c_{scr}(t)$ to form the multi-code DS-CDMA stream. In this paper, the

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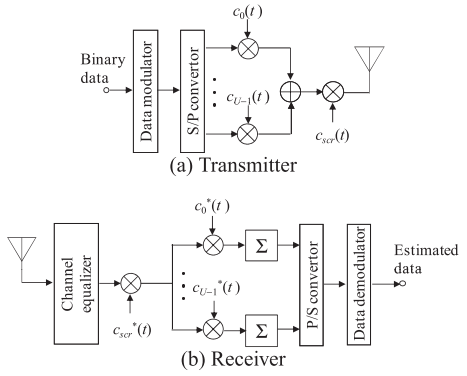

Fig. 1 System model of the multi-code DS-CDMA.

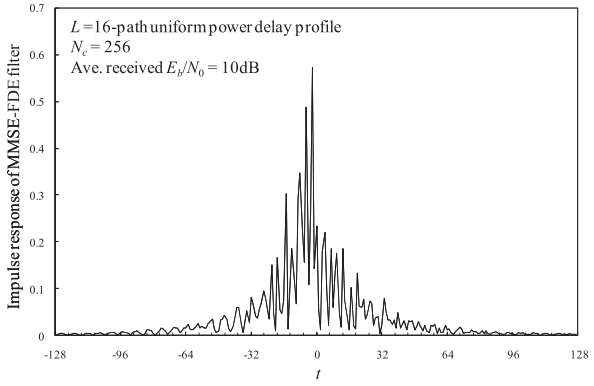

Fig. 2 Impulse response of MMSE-FDE filter.

chip-spaced discrete time representation is used.

The multi-code DS-CDMA signal to be transmitted is expressed as

$$s(t) = \sqrt{\frac{2E_c}{T_c}} \sum_{u=0}^{U-1} d_u(\lfloor t/SF \rfloor) c_{scr}(t) c_u(t \bmod SF), \quad (1)$$

where E_c and T_c denote the chip energy and chip duration, respectively, and $\lfloor x \rfloor$ represents the largest integer smaller than or equal to x.

The transmitted DS-CDMA signal is received via a frequency-selective channel. The received signal is expressed as

$$r(t) = \sum_{l=0}^{L-1} h_l s(t - \tau_l) + \eta(t), \quad (2)$$

where h_l is the lth complex-valued path gain with $\sum_{l=0}^{L-1} E[|h_l|^2] = 1$ ($E[.]$ denotes the ensemble average operation), and τ_l is the delay time of the lth path. $\eta(t)$ is a zero-mean complex-valued additive white Gaussian noise (AWGN) with a variance $2N_0/T_c$ with N_0 being the single-sided power spectrum density.

2.2 Overlap FDE

The residual IBI after MMSE-FDE is a circular convolution of the MMSE-FDE filter impulse response and the IBI.

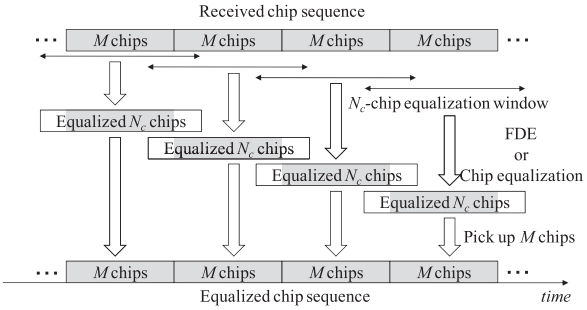

Fig. 3 Block signal processing of overlap FDE and SWCE.

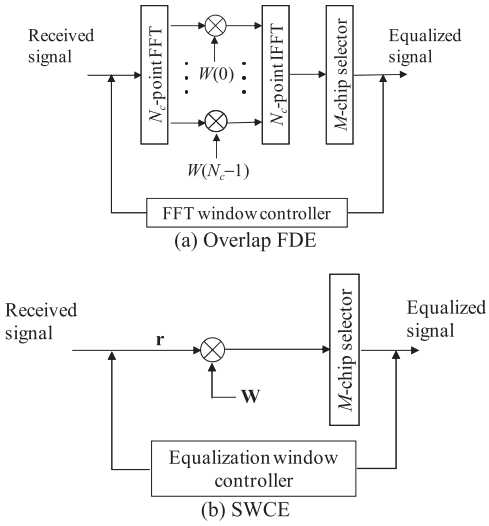

Fig. 4 Structure of the channel equalizer.

Since the IBI exists only over an interval of first $L-1$ chips of the received N_c-chip block and the impulse response of MMSE-FDE filter concentrates around $t = 0$ as shown in Fig. 2, the residual IBI is localized only near both ends of the equalized N_c-chip block. The overlap FDE exploits this fact.

The received DS-CDMA signal stream is divided into a sequence of M-chip blocks ($M \le N_c$). Then, N_c-point fast Fourier transform (FFT) is applied to an N_c-chip block centering the M-chip block of interest. After MMSE-FDE, the central M-chip block in the equalized N_c-chip block is picked up to suppress the residual IBI. The FFT intervals for consecutive M-chip blocks are overlapped as shown in Fig. 3.

Figure 4(a) shows the equalizer structure of overlap FDE. The received DS-CDMA signal vector $\mathbf{r} = [r(0), ..., r(N_c - 1)]^T$ over an N_c-chip interval can be expressed using the matrix form as

$$\begin{aligned} \mathbf{r} &= \mathbf{h}\mathbf{s}_0 + \boldsymbol{\nu} + \boldsymbol{\eta} \\ &= \mathbf{h}\mathbf{s}_0 + \mathbf{h}_{-1}(\mathbf{s}_{-1} - \mathbf{s}_0) + \boldsymbol{\eta}, \end{aligned} \quad (3)$$

where the first and second terms represent the desired signal component and the IBI component, respectively. $\mathbf{s}_0$, $\mathbf{s}_{-1}$ and $\boldsymbol{\eta}$ are respectively an $N_c \times 1$ vector given as

$$\begin{cases} \mathbf{s}_0 = [s(0), s(1), ..., s(N_c-1)]^T \\ \mathbf{s}_{-1} = [s(-N_c), s(-N_c+1), ..., s(-1)]^T \\ \boldsymbol{\eta} = [\eta(0), \eta(1), ..., \eta(N_c-1)]^T. \end{cases} \tag{4}$$

$\mathbf{h}$ and $\mathbf{h}_{-1}$ are $N_c \times N_c$ channel impulse response matrices given as

$$\begin{cases} \mathbf{h} = \begin{bmatrix} h_0 & & & h_{L-1} & \cdots & h_1 \\ \vdots & \ddots & & & \ddots & \vdots \\ \vdots & \vdots & h_0 & \mathbf{0} & & h_{L-1} \\ h_{L-1} & \vdots & \vdots & h_0 & & \\ & \ddots & \vdots & \vdots & \ddots & \\ \mathbf{0} & & h_{L-1} & h_{L-2} & \cdots & h_0 \end{bmatrix} \\ \mathbf{h}_{-1} = \begin{bmatrix} & h_{L-1} & \cdots & h_1 \\ & & \ddots & \vdots \\ & & & h_{L-1} \\ \mathbf{0} & & & \\ & & & \\ & & & \end{bmatrix}. \end{cases} \tag{5}$$

The received N_c-chip signal block of Eq. (3) is transformed by an N_c-point FFT into the frequency-domain signal $\mathbf{R} = [R(0), ..., R(N_c-1)]^T$. $\mathbf{R}$ is expressed as

$$\mathbf{R} = \mathbf{Fr} = \mathbf{H}(\mathbf{Fs_0}) + \mathbf{Fh}_{-1}(\mathbf{s}_{-1} - \mathbf{s}_0) + \mathbf{F}\boldsymbol{\eta}, \tag{6}$$

where $\mathbf{H} = \mathbf{FhF}^H$ with

$$\mathbf{F} = \frac{1}{\sqrt{N_c}} \begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & e^{-j2\pi\frac{1\cdot 1}{N_c}} & \cdots & e^{-j2\pi\frac{1\cdot(N_c-1)}{N_c}} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & e^{-j2\pi\frac{(N_c-1)\cdot 1}{N_c}} & \cdots & e^{-j2\pi\frac{(N_c-1)\cdot(N_c-1)}{N_c}} \end{bmatrix}, \tag{7}$$

being the $N_c \times N_c$ FFT matrix. Since $\mathbf{h}$ is a circulant matrix, $\mathbf{H}$ becomes an diagonal matrix, given by

$$\mathbf{H} = diag[H(0), ..., H(k), ..., H(N_c-1)], \tag{8}$$

where

$$H(k) = \sum_{l=0}^{L-1} h_l \exp\left(-j2\pi k \frac{\tau_l}{N_c}\right). \tag{9}$$

FDE is performed as $\hat{\mathbf{R}} = \mathbf{WR}$, where $\mathbf{W}$ is the MMSE-FDE weight matrix. $\hat{\mathbf{R}}$ can be expressed as

$$\hat{\mathbf{R}} = \mathbf{WH}(\mathbf{Fs}_0) + \mathbf{WFh}_{-1}(\mathbf{s}_{-1} - \mathbf{s}_0) + \mathbf{WF}\boldsymbol{\eta}, \tag{10}$$

where the first, second, and third terms are the desired signal, IBI, and noise, respectively. We want to derive the MMSE weight for the given $\mathbf{s}_0$ ($\mathbf{s}_{-1}$ is treated as a random vector), $\mathbf{h}$, and $\mathbf{h}_{-1}$. Since $\mathbf{s}_{-1}$ is independent of $\mathbf{s}_0$, $E[(\mathbf{Fh}_{-1}(\mathbf{s}_{-1} - \mathbf{s}_0))(\mathbf{Fh}_{-1}(\mathbf{s}_{-1} - \mathbf{s}_0))^H] = 2U(2E_c/T_c)(\mathbf{Fh}_{-1})(\mathbf{Fh}_{-1})^H$ for the given $\mathbf{h}_{-1}$. Therefore, according to the Wiener theory [12], $\mathbf{W}$ is obtained, for the given $\mathbf{h}$ and $\mathbf{h}_{-1}$, as

$$\mathbf{W} = \mathbf{H}^H \left\{ \mathbf{HH}^H + 2(\mathbf{Fh}_{-1})(\mathbf{Fh}_{-1})^H + \left(U\frac{E_c}{N_0}\right)^{-1} \mathbf{I} \right\}^{-1}. \tag{11}$$

By approximating $(\mathbf{Fh}_{-1})(\mathbf{Fh}_{-1})^H$ in Eq. (11) as a diagonal matrix, $\mathbf{W}$ can be expressed as a diagonal matrix, i.e., $\mathbf{W} = diag[W(0), ..., W(N_c-1)]$, resulting in one-tap MMSE-FDE. $W(k)$ is given by

$$W(k) = \frac{H^*(k)}{|H(k)|^2 + \sigma^2}, \tag{12}$$

and

$$\sigma^2 = \frac{2}{N_c} \sum_{l=0}^{L-1} |h_l|^2 \tau_l + \left(U\frac{E_c}{N_0}\right)^{-1} \tag{13}$$

is the IBI plus noise power normalized by the signal power [9]. Since we are assuming that the FFT window is synchronized to the $l = 0$th path, the last τ_l chips in the preceding block interfere with the present block and as a consequence, the IBI power contributed from the lth path is in proportion to instantaneous squared value of path gain times delay time, i.e., $|h_l|^2\tau_l$.

The frequency-domain signal after MMSE-FDE is transformed by an N_c-point inverse FFT (IFFT) back to the time-domain signal block as $\hat{\mathbf{r}} = \mathbf{F}^H\hat{\mathbf{R}}$. $\hat{\mathbf{r}}$ can be expressed as

$$\hat{\mathbf{r}} = \left(\frac{1}{N_c} tr[\mathbf{WH}]\right)\mathbf{s}_0 + \hat{\boldsymbol{\mu}} + \hat{\boldsymbol{\nu}} + \hat{\boldsymbol{\eta}}, \tag{14}$$

where the first term is the desired signal and $\hat{\boldsymbol{\mu}}$, $\hat{\boldsymbol{\nu}}$, and $\hat{\boldsymbol{\eta}}$ are the residual inter-chip interference (ICI), residual IBI, and noise component, respectively. $\hat{\boldsymbol{\mu}}$, $\hat{\boldsymbol{\nu}}$, and $\hat{\boldsymbol{\eta}}$ for overlap FDE are given, for the given $\mathbf{h}$ and $\mathbf{h}_{-1}$, as

$$\begin{cases} \hat{\boldsymbol{\mu}} = \left\{ \mathbf{F}^H(\mathbf{WH})\mathbf{F} - \left(\frac{1}{N_c} tr[\mathbf{WH}]\right)\mathbf{I} \right\}\mathbf{s}_0 \\ \hat{\boldsymbol{\nu}} = \mathbf{F}^H(\mathbf{WFh}_{-1})(\mathbf{s}_{-1} - \mathbf{s}_0) \\ \hat{\boldsymbol{\eta}} = \mathbf{F}^H(\mathbf{WF})\boldsymbol{\eta}. \end{cases} \tag{15}$$

To suppress the residual IBI, only the central M-chip block is picked up from the equalized N_c-chip block of Eq. (14) for the given value of N_c. Another way is to extend the FFT block size N_c for the given value of M.

2.3 SWCE

SWCE is a time-domain equalization technique [11]. Similar to the overlap FDE, the received DS-CDMA signal stream is divided into a sequence of M-chip blocks. Then, SWCE is applied to an N_c-chip block centering the M-chip block of interest, where N_c ($\geq M$) is the equalization block length. After the chip equalization, the central M-chip block is picked up from the equalized signal block of N_c chips

to suppress the residual IBI. To equalize the next M-chip block, an N_c-chip equalization window is shifted by M chips as shown in Fig. 3.

Figure 4(b) shows the equalizer structure of SWCE. The received signal block of N_c chips shown in Eq. (3) can be rewritten as

$$\mathbf{r} = (\mathbf{h} - \mathbf{h}_{-1})\mathbf{s}_0 + \mathbf{h}_{-1}\mathbf{s}_{-1} + \boldsymbol{\eta}. \tag{16}$$

The chip equalization is carried out on the received N_c-chip vector $\mathbf{r}$ as $\hat{\mathbf{r}} = \mathbf{w}\mathbf{r}$, where $\mathbf{w}$ is the $N_c \times N_c$ MMSE equalization weight matrix. By introducing

$$\mathbf{h}' = \mathbf{h} - \mathbf{h}_{-1} = \begin{bmatrix} h_0 & & & & & \mathbf{0} \\ \vdots & \ddots & & & & \\ \vdots & \vdots & h_0 & & & \\ h_{L-1} & \vdots & \vdots & h_0 & & \\ & \ddots & \vdots & \vdots & \ddots & \\ \mathbf{0} & & h_{L-1} & h_{L-2} & \dots & h_0 \end{bmatrix}, \tag{17}$$

$\hat{\mathbf{r}}$ can be expressed as

$$\hat{\mathbf{r}} = \mathbf{w}\mathbf{h}'\mathbf{s}_0 + \mathbf{w}\mathbf{h}_{-1}\mathbf{s}_{-1} + \mathbf{w}\boldsymbol{\eta}, \tag{18}$$

where the first, second, and third terms are the desired signal, IBI, and noise, respectively. Similar to the case of overlap FDE, we want to derive the MMSE weight for the given $\mathbf{s}_0$ ($\mathbf{s}_{-1}$ is treated as a random vector), $\mathbf{h}'$, and $\mathbf{h}_{-1}$. Since $\mathbf{s}_{-1}$ is independent of $\mathbf{s}_0$, $E[(\mathbf{h}_{-1}\mathbf{s}_{-1})(\mathbf{h}_{-1}\mathbf{s}_{-1})^H] = U(2E_c/T_c)\mathbf{h}_{-1}\mathbf{h}_{-1}^H$ for the given $\mathbf{h}_{-1}$. Therefore, according to the Wiener theory [12], $\mathbf{w}$ is obtained, for the given $\mathbf{h}'$ and $\mathbf{h}_{-1}$, as

$$\mathbf{w} = \mathbf{h}'^H \left\{ \mathbf{h}'\mathbf{h}'^H + \mathbf{h}_{-1}\mathbf{h}_{-1}^H + \left(U\frac{E_c}{N_0}\right)^{-1}\mathbf{I} \right\}^{-1}. \tag{19}$$

The diagonal elements in $\mathbf{w}\mathbf{h}'$ represents the equivalent channel gains after equalization for N_c chips in the desired signal block. Denoting $\hat{h}(n)$ is the equivalent channel gain (i.e., the nth diagonal element of $\mathbf{w}\mathbf{h}'$) for the nth chip in the signal block, Eq. (18) can be rewritten as

$$\hat{\mathbf{r}} = diag[\hat{h}(0), ..., \hat{h}(n), ..., \hat{h}(N_c - 1)]\mathbf{s}_0 + \hat{\boldsymbol{\mu}} + \hat{\boldsymbol{\nu}} + \hat{\boldsymbol{\eta}}, \tag{20}$$

where the first term is the desired signal block and $\hat{\boldsymbol{\mu}}$, $\hat{\boldsymbol{\nu}}$, and $\hat{\boldsymbol{\eta}}$ are the residual ICI, residual IBI, and noise component, respectively. $\hat{h}(n)$ can be expressed as

$$\hat{h}(n) = \sum_{q=0}^{N_c-1} (\mathbf{w})_{n,q}(\mathbf{h}')_{q,n}, \tag{21}$$

where $(\mathbf{w})_{p,q}$ and $(\mathbf{h}')_{p,q}$ are the (p, q) element of $\mathbf{w}$ and $\mathbf{h}'$, respectively. $\hat{\boldsymbol{\mu}}$, $\hat{\boldsymbol{\nu}}$, and $\hat{\boldsymbol{\eta}}$ for SWCE are given, for the given $\mathbf{h}'$ and $\mathbf{h}_{-1}$, as

Table 1 No. of complex multiply operations per symbol.

		No. of complex multiply operations per symbol
SWCE	Weight generation	$4N_c^3(SF/UM)$
	Chip equalization	$N_c^2(SF/UM)$
	Total	$(4N_c^3+N_c^2)(SF/UM)$
Overlap FDE	N_c-point FFT	$(N_c\log_2 N_c)(SF/UM)$
	Weight generation	$2N_c(SF/UM)$
	FDE	$N_c(SF/UM)$
	N_c-point IFFT	$(N_c\log_2 N_c)(SF/UM)$
	Total	$N_c(3+2\log_2 N_c)(SF/UM)$

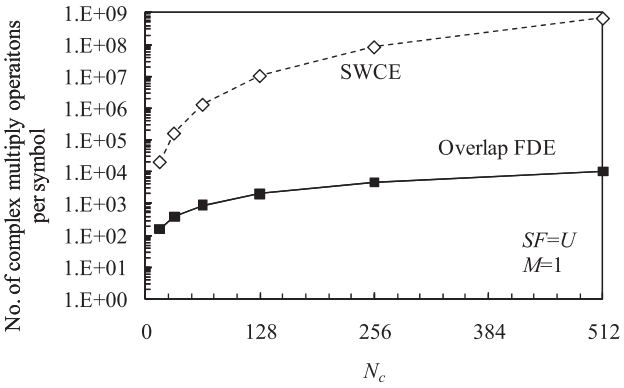

Fig. 5 Complexity comparison.

$$\begin{cases} \hat{\boldsymbol{\mu}} = \left\{\mathbf{w}\mathbf{h}' - diag[\hat{h}(0), ..., \hat{h}(n), ..., \hat{h}(N_c - 1)]\right\}\mathbf{s}_0 \\ \hat{\boldsymbol{\nu}} = \mathbf{w}\mathbf{h}_{-1}\mathbf{s}_{-1} \\ \hat{\boldsymbol{\eta}} = \mathbf{w}\boldsymbol{\eta}. \end{cases} \tag{22}$$

After the chip equalization, similar to overlap FDE, only the central M-chip block in $\hat{\mathbf{r}}$ is picked up.

2.4 Computational Complexity

SWCE is a time-domain equalization using a matrix computation and therefore, its computational complexity is very large. On the other hand, the complexity of overlap FDE is much smaller than SWCE. Table 1 compares SWCE and overlap FDE in terms of the number of complex multiply operations per symbol. In the case of SWCE, the number of multiply operations is in proportion to N_c^3 due to the inverse matrix computation in Eq. (19) and therefore, the complexity significantly increases with N_c. The complexity comparison between overlap FDE and SWCE is shown in Fig. 5. Overlap FDE requires much less complexity than SWCE. When $N_c = 128$, the number of multiply operations per symbol is approximately 10^7 for SWCE and 2×10^3 for overlap FDE.

3. Computer Simulation

Table 2 summarizes the simulation condition. We assume uncoded QPSK transmission. The propagation channel is assumed to be a frequency-selective block Rayleigh fading channel having a chip-spaced $L = 16$-path exponential power delay profile with decay factor α. The ideal channel

Table 2 Simulation condition.

Transmitter	Data modulation	QPSK
	Spreading sequence	Product of Walsh sequence and Long PN sequence
	Spreading factor	$SF = 16$
	Code multiplexing order	$U = 1 \sim SF$
Channel model	Frequency-selective block Rayleigh fading	
	Power delay profile	L=16-path exponential
	Decay factor	α=0, 6dB
	Delay time	$\tau_l = l$ (chip-spaced)
Receiver	Equalization	Overlap FDE, SWCE
	Channel estimation	Ideal

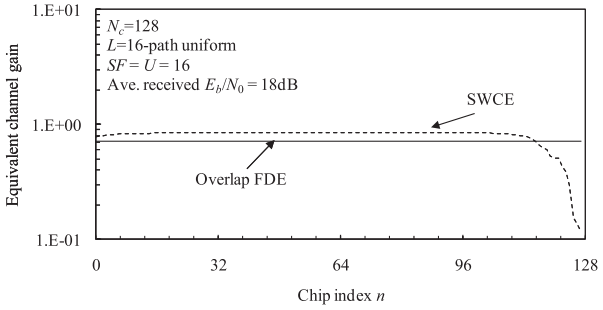

Fig. 6 Equivalent channel gain.

estimation is also assumed.

Figure 6 shows the amplitude of the equivalent channel gain for the nth chip in the $N_c = 128$-chip block for $\alpha = 0$ dB (uniform power delay profile). The equivalent channel gain for the nth chip is given as

$$\hat{h}(n) = \begin{cases} \dfrac{1}{N_c} tr[\mathbf{WH}] & \text{for Overlap FDE} \\ \displaystyle\sum_{q=0}^{N_c-1} (\mathbf{w})_{n,q} (\mathbf{h}')_{q,n} & \text{for SWCE.} \end{cases} \tag{23}$$

As seen from Fig. 6, in the case of overlap FDE, the equivalent channel gain is same at all chip positions. On the other hand, in SWCE, the amplitude of the equivalent channel gain drops near the end of the N_c-chip block. The reason for this is expressed below. Assuming that the SWCE window is synchronized to the $l = 0$th path, the last τ_l chips in the chip block received via the lth path spill out of the SWCE window. As a result, the full (the Lth order) path diversity gain cannot be obtained near the end of chip block.

Figure 7 plots the residual ICI and IBI power normalized by the signal power as a function of chip position n in an $N_c = 128$-chip block for $\alpha = 0$ dB. The residual ICI and IBI power are given as the diagonal element of $(1/2)E[\hat{\boldsymbol{\mu}}\hat{\boldsymbol{\mu}}^H]$ and $(1/2)E[\hat{\boldsymbol{\nu}}\hat{\boldsymbol{\nu}}^H]$, respectively. In the case of overlap FDE, $E[\hat{\boldsymbol{\mu}}\hat{\boldsymbol{\mu}}^H]$ and $E[\hat{\boldsymbol{\nu}}\hat{\boldsymbol{\nu}}^H]$ are derived using Eq. (15) as

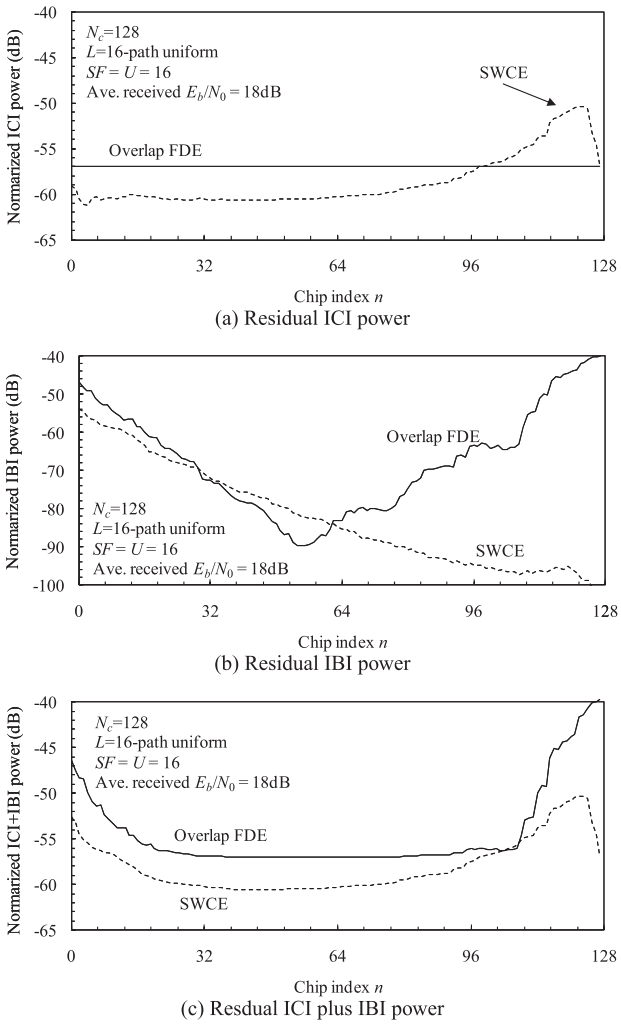

Fig. 7 Residual ICI and IBI powers.

$$\begin{cases} E[\hat{\boldsymbol{\mu}}\hat{\boldsymbol{\mu}}^H] = U\dfrac{2E_c}{T_c}\tilde{\mathbf{h}}\tilde{\mathbf{h}}^H \\ E[\hat{\boldsymbol{\nu}}\hat{\boldsymbol{\nu}}^H] = 2U\dfrac{2E_c}{T_c}\hat{\mathbf{w}}\mathbf{h}_{-1}(\hat{\mathbf{w}}\mathbf{h}_{-1})^H, \end{cases} \tag{24}$$

where

$$\begin{cases} \tilde{\mathbf{h}} = \hat{\mathbf{w}}\mathbf{h} - \left(\dfrac{1}{N_c} tr[\mathbf{WH}]\right)\mathbf{I} \\ \hat{\mathbf{w}} = \mathbf{F}^H\mathbf{WF}. \end{cases} \tag{25}$$

In the case of SWCE, they are respectively derived using Eq. (22) as

$$\begin{cases} E[\hat{\boldsymbol{\mu}}\hat{\boldsymbol{\mu}}^H] = U\dfrac{2E_c}{T_c}\tilde{\mathbf{h}}'\tilde{\mathbf{h}}'^H \\ E[\hat{\boldsymbol{\nu}}\hat{\boldsymbol{\nu}}^H] = U\dfrac{2E_c}{T_c}\mathbf{w}\mathbf{h}_{-1}(\mathbf{w}\mathbf{h}_{-1})^H, \end{cases} \tag{26}$$

where

$$\tilde{\mathbf{h}}' = \mathbf{w}\mathbf{h}' - \left(diag[\hat{h}(0), ..., \hat{h}(n), ..., \hat{h}(N_c - 1)]\right)\mathbf{I}. \tag{27}$$

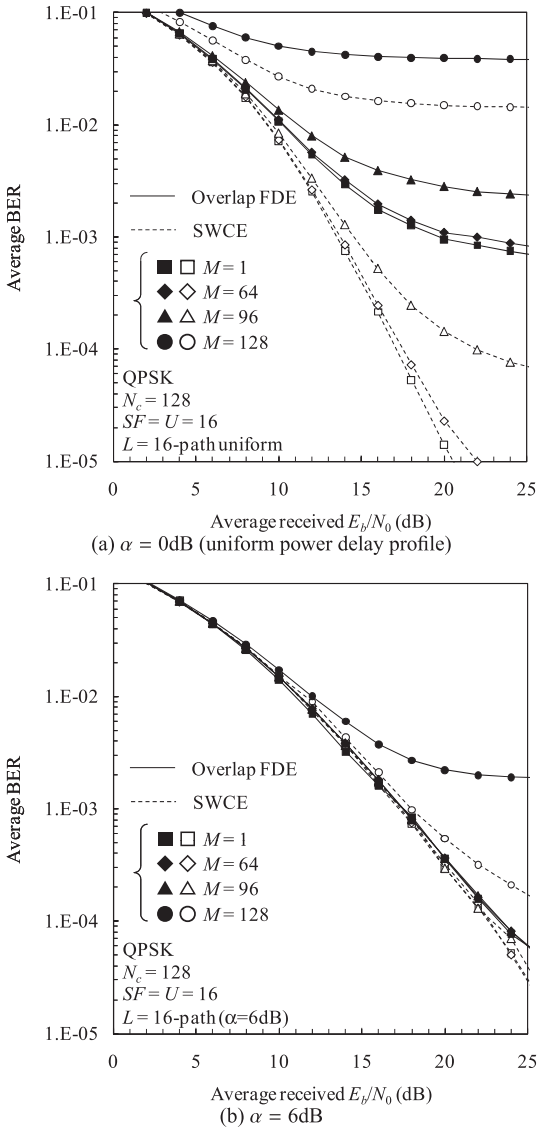

Fig. 8 BER performance comparison for various values of M. N_c =128.

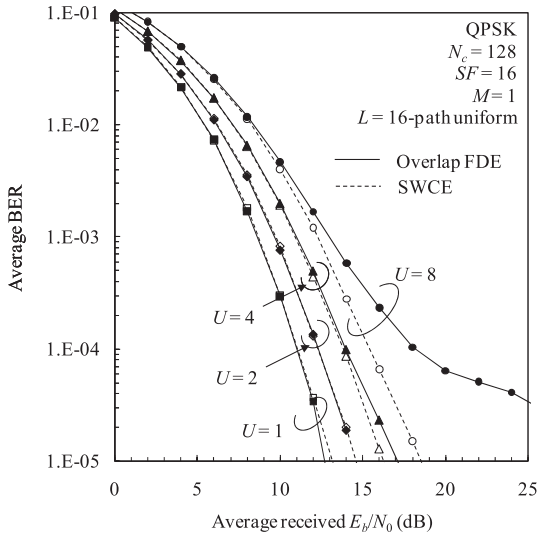

Fig. 9 Impact of U.

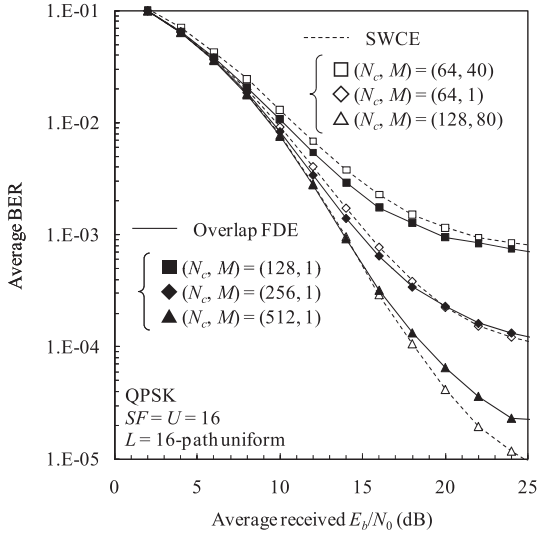

Fig. 10 BER performance comparison for various (N_c, M).

As seen from Figs. 7(a) and (b), SWCE has smaller residual ICI power than overlap FDE except near the end of N_c-chip block. On the other hand, SWCE has smaller residual IBI power than overlap FDE in the latter half of N_c-chip block. Figure 7(c) plots the residual ICI plus IBI power normalized by the signal power as a function of chip position n. It can be seen from Fig. 7(c) that overlap FDE has larger residual ICI plus IBI power than SWCE. This suggests that for the same chip block size, overlap FDE is inferior to SWCE even if small M is used.

Figure 8 plots the BER performances of overlap FDE and SWCE as a function of the average bit energy-to-noise power spectrum density ratio E_b/N_0 (= $0.5SF(E_c/N_0)$) with M as a parameter. N_c = 128 is assumed. When α = 0 dB (uniform power delay profile), smaller M can provide better BER performance for both overlap FDE and SWCE (see Fig. 8(a)). However, overlap FDE is inferior to SWCE even if small M is used. This is because the residual ICI plus IBI is larger with overlap FDE than with SWCE over an M-chip block (see Fig. 7(c)). When the channel frequency-selectivity is weak (α = 6 dB), the residual ICI and residual IBI becomes small and therefore, overlap FDE can achieve almost the same BER performance as SWCE except for $N_c = M$.

Figure 9 plots the BER performance with the code multiplexing order U as a parameter when M = 1. When U is small, the BER performance of both overlap FDE and SWCE improves and overlap FDE can be achieve almost the same performance as SWCE. However, as U increases, the residual ICI and IBI becomes larger (see Eqs. (24) and (26)) and therefore, the performance of overlap FDE becomes worse than SWCE.

Overlap FDE can suppress more the residual ICI and residual IBI by increasing N_c while using the same value of M. Figure 10 plots the BER performances of overlap FDE

with N_c = 128, 256 and 512 when M = 1. For comparison, also plotted in Fig. 10 are the BER performances of SWCE with (N_c, M) = (64, 40), (64, 1) and (128, 80). The above settings (Nc, M) = (64, 80), (64, 1) and (128, 80) for SWCE are chosen so that almost the same BER performance can be achieved as overlap FDE using (N_c, M) = (128, 1), (256, 1) and (512, 1), respectively, while minimizing the computational complexity. It can be seen from Fig. 10 that the BER performance of overlap FDE improves as N_c increases. Overlap FDE with N_c = 128, 256 and 512 can achieve almost the same performance as SWCE using (N_c, M) = (64, 40), (64, 1) and (128, 80), respectively. When N_c = 128, 256 and 512, the number of multiply operations per symbol is about 2×10^3, 5×10^3, and 1×10^4, respectively, for overlap FDE while it is 3×10^4, 1×10^6, and 1×10^5, respectively, for SWCE using (N_c, M) = (64, 40), (64, 1) and (128, 80). As a consequence, overlap FDE can achieve almost the same performance as SWCE with much less complexity.

4. Conclusion

In this paper, we compared overlap FDE and SWCE in terms of the BER performances and computational complexity for multi-code DS-CDMA. The residual interference after equalization is localized only near the both ends of the equalized chip block and, therefore, it can be suppressed by picking up only the central M chips. However, in the case of overlap FDE, the residual IBI within the M-chip block gets stronger as the channel frequency-selectivity gets stronger and the BER performance degrades. On the other hand, by extending the FFT block size, overlap FDE can achieve almost the same performance as SWCE with much less complexity than SWCE.

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